

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claims 1-4 (Canceled).

Claim 5 (Previously presented): A switching apparatus for receiving and transmitting frames and messages, wherein the frames consist of relatively long strings of bytes and the messages consist of small entities, the switching apparatus comprising

    a ring of plural data ports comprising input ports and output ports, wherein each data port is interconnected to two adjacent data ports, the ring defining for any given pairing of one input port and one output port a set of zero or more intermediate data ports in a given direction, the ring for passing the messages received at the input ports through any respective intermediate ports to designated output ports

    a crossbar for switching the frames from the input ports to the output ports  
    wherein the frames and messages are processed simultaneously.

Claim 6 (Previously presented): The switching apparatus of claim 5 further comprising  
    a parser for separating the frames from the messages to form two separate data streams.

Claim 7 (Previously presented): The switching apparatus of claim 5 further comprising  
    a clock for moving the messages by one data port for every clock pulse.

Claim 8 (Previously presented): The switching apparatus of claim 5 further comprising plural gates respectively associated with each data port for allowing a given message into a given data port only if no other data is present in the given data port.

Claim 9 (Previously presented): The switching apparatus of claim 5 further comprising a controller for preventing conflict between message passing on the ring and switching by the crossbar.

Claim 10 (Previously presented): A process for receiving and transmitting frames and messages, wherein the frames consist of relatively long strings of bytes and the messages consist of small entities, the process comprising interconnecting plural data ports in a ring, the data ports comprising input ports and output ports, wherein each data port is interconnected to two adjacent ports, the ring defining for any given pairing of one input port and one output port a set of zero or more intermediate data ports in a given direction

passing the messages received at the input ports around the ring through any respective intermediate ports to designated output ports

simultaneously with passing the messages, switching the frames from the input ports to the output ports via a crossbar.

Claim 11 (Previously presented): The process of claim 10 further comprising separating the frames from the messages to form two separate data streams.

Claim 12 (Previously presented): The process of claim 10 further comprising  
moving the messages by one data port for every clock pulse.

Claim 13 (Previously presented): The process of claim 10 further comprising  
allowing a given message into a given data port only if no other data is present in the  
given data port.

Claim 14 (Previously presented): The process of claim 10 further comprising  
preventing conflict between message passing on the ring and switching.

Claim 15 (Currently amended): Apparatus for receiving and transmitting frames and messages,  
wherein the frames consist of relatively long strings of bytes and the messages consist of small  
entities, the process apparatus comprising

means for interconnecting plural data ports in a ring, the data ports comprising input ports  
and output ports, wherein each data port is interconnected to two adjacent ports, the ring defining  
for any given pairing of one input port and one output port a set of zero or more intermediate data  
ports in a given direction

means for passing the messages received at the input ports around the ring through any  
respective intermediate ports to designated output ports

means for, simultaneously with passing the messages, switching the frames from the  
input ports to the output ports via a crossbar.

Claim 16 (Previously presented): The apparatus of claim 15 further comprising  
means for separating the frames from the messages to form two separate data streams.

Claim 17 (Previously presented): The apparatus of claim 15 further comprising  
means for moving the messages by one data port for every clock pulse.

Claim 18 (Previously presented): The apparatus of claim 15 further comprising  
means for allowing a given message into a given data port only if no other data is present  
in the given data port.

Claim 19 (Previously presented): The apparatus of claim 15 further comprising  
means for preventing conflict between message passing on the ring and switching.

Claim 20 (Previously presented): A process for receiving and transmitting frames and messages,  
wherein the frames consist of relatively long strings of bytes and the messages consist of small  
entities, the process comprising  
determining whether a data packet is a message or frame  
if the data packet is a frame, then routing the frame through a crossbar switch  
if the data packet is a message, then  
inserting the message into one of a plurality of ports, wherein the ports are  
interconnected in a ring  
giving the message a message ring destination identifier  
passing the message from port to port until the message reaches a destination port.

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Claim 21 (Currently amended): The process of claim 20 further comprising  
if the data packet is a message, then placing the message in a message-in queue.

Claim 22 (Previously presented): The process of claim 21  
wherein the message-in queue comprises a FIFO.

Claim 23 (Previously presented): The process of claim 20 further comprising  
after the message reaches the destination port, placing the message in a message-out  
queue.

Claim 24 (Previously presented): The process of claim 23  
wherein the message-out queue comprises a FIFO.